Remarks

Thorough examination by the Examiner is noted and appreciated.

Claims 5 and 16 have been amended to correct a grammatical error and as required by Examiner to overcome Examiners objection and rejection under Section 112.

Claim Objections

Claim 5 has been amended to overcome Examiner objection.

Claim Rejections under 35 USC 112

Claim 5 has been amended to overcome Examiners rejection.

With respect to claim 13, Applicants respectfully point out

that Examiner is mistaken; "about 10" has been lined through ("~~about 10~~" i.e., deleted) in Applicants amendment of 2/28/2006. Perhaps Examiner is referring to an imaged version of Applicants amendment which may not clearly show the line-through in the imaged version.

Claim Rejections under 35 USC 103

1. Claims 1-2, 4, 6, 9, 13, 17, 19, 21, and 22 stand rejected under 35 USC 103(a) as being unpatentable over Labelle et al. (20050101147) in view of Loan et al. (6, 136, 725).

Labelle et al. appears to be an improperly used reference as it has a filing date of 11/8/2003, after the filing date of Applicants instant Application of 10/01/2003.

Thus, while noting Labelle et al. is an improperly used reference, Applicants nevertheless point out important differences between Labelle et al. and Applicants disclosed and claimed invention.

Labelle et al. discloses a nitridation process performed on

a gate stack (interfacial layer/high-K layer/gate electrode layer) with a single high-K dielectric segment (see paragraph 0012). In addition, Labelle et al. discloses that the interfacial layer comprises nitride (paragraph 0015). In addition, Labelle et al. teach that the nitridation of the gate stack using a nitrogen plasma, **nitridates the sidewalls of the gate stack and repairs damage** that may occur to the gate stack during etching and that it forms an **oxygen diffusion barrier on the sidewalls** to prevent lateral oxygen diffusion in subsequent process steps (paragraph 0014, 0015). Further, Labelle et al. teach that a rapid thermal anneal process may be performed following formation of sidewall spacers and ion implantation to form source drain regions (paragraph 0016).

Labelle et al. nowhere suggest or disclose Applicants disclosed and claimed invention or recognize or suggest a solution to the problem that Applicants have recognized and solved:

"A method for treating a gate structure **comprising a high-K gate dielectric stack to reduce interface states between a high-K gate dielectric and a gate electrode**"

Examiner further erroneously states that Labelle et al. disclose a process **to reduce interface states between a high-K gate dielectric and a gate electrode** and refers to paragraph 0017 which nowhere discloses or suggest such a result or process.

With respect to claim 2, Examiner is further mistaken that Labelle et al. disclose an annealing step following the plasma treatment, rather, Labelle et al. disclose a rapid thermal anneal following an ion implantation step.

Examiner admits that Labelle does not teach a gate dielectric stack.

Since Labelle is an improperly used reference, Examiners combination of other references is not further addressed, including the combination of Loan et al. who teach:

"A method for chemical vapor deposition includes dispensing a precursor to a vaporizer positioned within a vaporization chamber and delivering a vapor to a process chamber **without a carrier gas.**" (see Abstract)

"Further, the methods and apparatus of this invention are suitable for the deposition of **stacked gate dielectrics,** which include successively deposited layers of extremely thin films (on the order of 15 angstroms for each film) of **two different dielectrics to minimize gate capacitance.** Stacked dielectric

gates may generally be used in devices with geometries of less than 0.15 microns and in devices with geometries of up to 0.25 microns where an increase in speed beyond 400 MHZ is needed."(see col 25, lines 35-43).

2. Claims 3, and 14-15 stand rejected under 35 USC 103(a) as being unpatentable over Labelle et al. in view of Loan et al. , above and further in view of Wolf (silicon Processing for the VLSI Era, Volume 1, Process Technology; page 58, para. 2, 1986, Lattice Press (ISBN 0-9616721-3-7).

Applicants reiterate the comments made above with respect to Labelle et al. and Loan et al.

Applicants note that Wolf disclose that RTP systems are conventionally used in semiconductor processing and that heating is typically done in inert atmospheres including Ar or N2 or vacuum may be used or oxygen or ammonia for growth of SiO2 and Si3N4 (page 58, first paragraph) as well as generally disclosing that temperatures may range from 420 to 1150 °C, depending of the process, and further note that RTP is used to activate dopants after ion implantation and that new applications for the technique are constantly being discovered (3d paragraph).

3. Claims 5, 7, 16, and 18 stand rejected under 35 USC 103(a) as being unpatentable over Labelle et al. in view of Loan et al.

, above and further in view of Shinriki et al. (2005/0074983).

Applicants reiterate the comments made above with respect to Labelle et al. and Loan et al.

Applicants note that Shinriki et al. teach an apparatus for atomic layer deposition and further teach:

[0006] In order to form such a high-K dielectric gate insulation film on a Si substrate, there is a need of forming an SiO.sub.2 film having a thickness 1 nm or less, typically 0.8 nm or less, on the Si substrate as a base oxide film so as to suppress diffusion of metal elements constituting a high-K dielectric gate insulation film into the Si substrate, and then form a high-K dielectric gate insulation film on such extremely thin SiO.sub.2 base oxide film. Thereby, the high-K dielectric gate insulation film has to be formed such that the film does not contain defects such as interface states. Further, at the time of forming such a high-K dielectric gate insulation film on the base oxide film, it is preferable to change the composition thereof gradually from the composition primarily of SiO.sub.2 to the composition primarily of the high-K dielectric, from the side thereof contacting with the base oxide film toward the principal surface of the high-K dielectric gate insulation film.

[0007] In order to form the high-K dielectric gate insulation film such that it does not contain defects, it is not possible to use plasma process that involves the process of charged particles. For example, when such a high-K dielectric gate insulation film is formed by a plasma CVD process, there are formed defects that function as the trap of hot carriers within the film as a result of the plasma damages.

3. Claims 11 and 20 stand rejected under 35 USC 103(a) as being

unpatentable over Labelle et al. in view of Loan et al. , above and further in view of Steger (5.085,727).

Applicants reiterate the comments made above with respect to Labelle et al. and Loan et al.

Applicants note that Steger generally teach a **plasma etcher** may operated over a broad range of pressures depending on the plasma etcher.

Conclusion

The cited primary reference of Labelle et al. is an improper reference; therefore Examiner has failed to make out a *prima facie* case of obviousness with respect to Applicants independent claims, and therefore Applicants dependent claims.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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